UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,543	08/04/2000	Rajendra K. Talluri	TI-28919	1760

23494 7590 09/07/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	**PAPER NUMBER**
2622	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/632,543
Filing Date: August 04, 2000
Appellant(s): TALLURI ET AL.

Carlton H. Hoel
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/20/2006 appealing from the Office action mailed 3/23/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,597,394	Duncan et al.	7-2003
Re.36,338	Fukuoka	10-1999
6,642,956	Safai	11-2003

6,674,464 Mizutani et al. 1-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Duncan et al. (US 6,597,394).

Regarding claim 1, Duncan et al. discloses an integrated circuit for a digital still camera, comprising:

a first programmable processor programmed (microprocessor 202, figure 2, column 4, lines 1-33) to run control functions, said first processor coupled to a user interface (display 210, figure 2), a controller for memory (controller for memory 203, figure 2, column 1, lines 1-33), and a controller for image acquisition (image sensor 106, figure 2);

a second programmable processor (programmable addressing block 410 included in image transform processor 206 which performs compression operation, figures 2, 4, column 5, line 60 – column 6, line 31) programmed to run image processing and compression functions, said second processor coupled to said first processor (figure 2 shows that image transform processor 206 coupled to microprocessor 202);

a third processor coupled (arithmetic block 450, figure 4) to said second processor (programmable addressing block 410, figure 2), said third processor including at least four parallel multiply and accumulate units (arithmetic block 450 includes four multipliers 630-633 which is coupled to latches 640-643, figure 6A, column 15, lines 15-62).

Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Fukuoka (US Re. 36,338).

Regarding claim 4, Fukuoka discloses an integrated circuit for a digital still camera, comprising a first programmable processor programmed (CPU 11, figure 1, column 4, lines 17-39) to run control functions, said first processor coupled to a user interface (display section 19 and operating section 20, figure 1, column 4, lines 57-62), a controller for memory (CPU 11, figure 1, column 4, lines 36-39), and a controller for image acquisition (CPU 11, figure 1, column 4, lines 35-39); and a second programmable processor (compress and extending image data 7, figure 1, column 4, lines 30-39) programmed to run image processing and compression functions, said second processor coupled to said first processor (figure 1 shows that the compress and extending image data 7 is coupled to CPU 11); a digital image processing unit (digital signal processing 6, figure 1) separate from said first and second processors, said image processing unit arranged for real-time image sequence (video) processing, said image processing unit controlled in real-time by said first processor.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Safai (U S 6,642,956) in view of Mizutani et al. (U S 6,674,464).

Regarding claim 3, Safai discloses an integrated circuit for a digital still camera, comprising a first programmable processor programmed (microprocessor 312, figure 3, column 7, lines 7-28) to run control functions, said first processor coupled to a user interface (display 318 and touch screen 319, figure 1), a controller for memory (display controller 317, figure 1), and a controller for image acquisition (image capture unit 302); and a second programmable

processor (digital image processor 310, figure 3, column 5, lines 45-58) programmed to run image processing (performing some processing of digital images, column 5, lines 50-54) and compression functions (digital compressor 426, figure 4, column 9, lines 43-55), said second processor coupled to said first processor (figure 3 shows that digital image processor 310 coupled to microprocessor 312).

Safai fails to specifically disclose an image compression unit separate from said second processor, said compression unit arranged to compress acquired images for storage in a memory and to decompress said compressed acquired images in said memory for restorage in said memory. However, Mizutani et al. discloses a digital still camera 1 includes compression/expansion circuit 29, which is separated from memory controller 22, compresses image data to store in image memory 32, and expands the compressed image data (figures 2-3, column 6, lines 25-30). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Safai by the teaching of Mizutani et al. in order to compress image data before storing image data into a memory. This increases the amount of image data to be stored in the memory.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 6,597,394) in view of Fukuoka (U S Re. 36,338).

Regarding claim 5, Duncan et al. fails to specifically disclose an audio input coupled to said second processor, said second processor programmed to decode audio and said first processor programmed to output said decoded audio. However, Fukuoka discloses an electric still camera includes microphone 12 for inputting sound, microphone 12 is coupled to the sound

data compressing-extending circuit 15 (second processor). The sound data are extended by the sound data compressing-extending circuit 15, and outputted as an audio signal through D/A 22 and amplifier 23 by the control of central processing 11 (first processor), figure 1, column 5, lines 4-9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Duncan et al. by the teaching of Fukuoka in order to record sound data together with image data.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 6,597,394) in view of Safai (US 6,642,956) further in view of Mizutani et al. (US 6,674,464).

Regarding claim 6, Duncan fails to specifically disclose camera peripherals including USB, and compact flash/smart media interface.

However, Safai discloses a digital camera, which comprises camera peripherals including USB, and compact flash/smart media interface (USB port, PCMCIA port, figure 3, column 7, lines 13-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Duncan et al. by the teaching of Safai in order to use only one cable (USB) to transmit data and power. This reduces cost of the device.

Duncan et al. and Safai fail to specifically disclose camera peripherals including IrDA, NTSC/PAL encoder. However, Mizutani et al. discloses a digital still camera 1 includes an NTSC/PAL encoder 23, and IrDA interface 45 (figure 2, column 5, lines 39-40, column 6, lines 53-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the device in Duncan et al. and Safai by the teaching of Mizutani et al. in order to display image data on a TV monitor.

(10) Response to Argument

In re page 3, Appellants argue that the cited multipliers plus latches of Duncan do not suggest the four parallel multiply and accumulate units because there is no accumulation for each multiplier.

In response, regarding claim 1, it is noted that the feature "accumulation for each multiplier" is not claimed. Instead, claim 1 recites the limitation "said third processor including at least four parallel multiply and accumulate units." The examiner considers that Duncan et al. does disclose this limitation. Duncan et al. discloses that the arithmetic block 450, which corresponds to the third processor, can perform four multiply accumulates on each block cycle or phase, column 15, lines 28-29. Further, since a latch is used for holding (accumulating or storing) data, each combination of multiplier 630 and latch 640, or multiplier 631 and latch 641, or multiplier 632 and latch 642, or multiplier 633 and latch 643, each is considered as a "multiply and accumulate unit." Therefore, the arithmetic block 450, which includes four parallel multipliers 630-633 coupled to latches 640-643 (Duncan et al., figure 6A, lines 15-62) read on the limitation "said third processor including at least four parallel multiply and accumulate units."

In re page 3, Appellants argue that claim 4 requires a programmable second processor

for image compression; whereas, Fukuoka only describes CPU 11 as doing various tasks (i.e.. programmable) but does not suggest any programmability of compression circuit 7.

In response, the Examiner disagrees. Since the compression circuit 7 receives control operation from CPU 11 (a programmable processor), the compression circuit is programmable in order to receive control operation from CPU 11. Therefore, the compression circuit 7 is also considered as a programmable processor.

In re page 4, Appellants argue that claim 3 requires first and second processors plus a separate image compression unit; whereas Safai has image compression already in image processor 310, and there is no suggestion to include another unit for image compression.

In response, the Examiner disagrees. The digital image processor 310 in Safai only has compression functions performed by digital compressor 426 (see figures 3, 4, column 5, lines 45-58, column 9, lines 43-55). The digital compressor 426 does not perform the decompress function. Therefore, Safai does not disclose an image compression unit arranged to compress acquired images for storage in a memory and to decompress said compressed acquired images in said memory. However, Mizutani et al. discloses a digital still camera 1 that includes compression/expansion circuit 29, which is separated from memory controller 22, compresses image data to store in image memory 32, and expands the compressed image data (figures 2-3, column 6, lines 25-30). The compression/expansion circuit 29 expands the image data read out from the recording device 51 for displaying on finder 36 (figure 3, column 16, lines 11-34).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Safai by the teaching of Mizutani et al. in order to

compress image data before storing image data into a memory. This increases the amount of image data to be stored in the memory, and due to the expanded image data created by a compression/expansion circuit, the user can review more images on a display.

In re page 4, Appellants argue that claim 3 requires the compression unit be able to act on the acquired images, in contrast, Mizutani Fig.2 shows JPEG unit 29 applies after input processing 21 and thus does not act on the acquired image. Application Fig.1b shows burst mode compression/decompression unit 108 directly connected to the CCD controller to get the acquired image.

In response, regarding claim 3, it is noted that the features upon which appellants relies (i.e., Application Fig.1b shows burst mode compression/decompression unit 108 directly connected to the CCD controller to get the acquired image) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Instead, Appellants only recited the limitation "to compress acquired images for storage in a memory". Therefore, the limitation "acquired images" can be read as images before compressing by JPEG encoder/decoder 29 (figure 2, column 5, lines 45-52).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Luong T. Nguyen LN

DAVID OMETZ
SUPERVISORY PATENT EXAMINER

Conferees:

David Ometz, SPE Art Unit 2622

NgocYen Vu, SPE Art Unit 2622

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER

TEXAS INSTRUMENTS INCORPORATED
PO Box 655474, M/S 3999
Dallas, Texas 75265